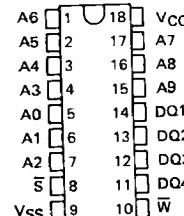


- Previously Celled TMS4045/TMS40L45
- 1024 X 4 Organization
- Single +5-V Supply
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

TMS2114, TMS2114L . . . NL PACKAGE
(TOP VIEW)

ACCESS READ OR WRITE

	TIME (MAX)	CYCLE (MIN)
TMS2114-15, TMS2114L-15	150 ns	150 ns
TMS2114-20, TMS2114L-20	200 ns	200 ns
TMS2114-25, TMS2114L-25	250 ns	250 ns
TMS2114-45, TMS2114L-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity with Standard TTL Loads - No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)
TMS2114	550 mW
TMS2114L	330 mW

PIN NOMENCLATURE	
A0 - A9	Addresses
DQ1 - DQ4	Data In/Data Out
S	Chip Select
VCC	+5-V Supply
VSS	Ground
W	Write Enable

description

This series of static random-access memories is organized as 1024 words of 4 bits each. Static design results in reducing overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship.

The TMS2114/2114L series is offered in the 18-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0 – A9)

The ten address inputs select one of the 1024 4-bit words in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select (\bar{S})

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

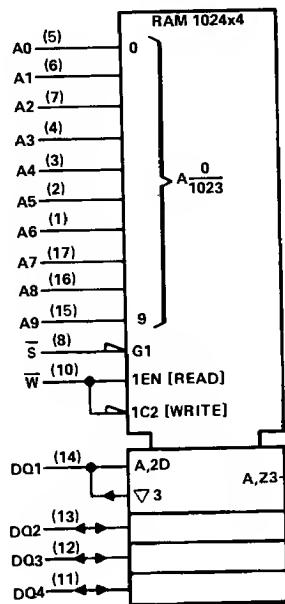
write enable (\bar{W})

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. \bar{W} or \bar{S} must be high when changing addresses to prevent erroneously writing data into a memory location. The \bar{W} input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1 – DQ4)

Data can be written into a selected device when the write enable input is low. The DQ terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The DQ terminals are in the high-impedance state when chip select (\bar{S}) is high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

logic symbol[†]



FUNCTION TABLE			
\overline{W}	\overline{S}	DQ1 – DQ4	MODE
L	L	VALID DATA	WRITE
H	L	DATA OUTPUT	READ
X	H	HI-Z	DEVICE DISABLED

[†]This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage, V_{CC} (see Note 1)	–0.5 V to 7 V
Input voltage (any input) (see Note 1)	–1 V to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–55°C to 150°C

[†]Stresses beyond those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground material.

recommended operating conditions

PARAMETER	TMS2114 TMS2114L			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}	0			V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)	–1		0.8	V
Operating free-air temperature, T_A	0	70		°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]			MIN	TYP [‡]	MAX	UNIT	
V _{OH} High-level voltage	I _{OH} = -1 mA	V _{CC} = MIN (operating)		2.4			V	
V _{OL} Low-level voltage	I _{OL} = 3.2 mA	V _{CC} = MIN (operating)			0.4		V	
I _I Input current	V _I = 0 V to MAX					10	μA	
I _{OZ} Off-state output current	S at 2 V or W at 0.8 V	V _O = 0 V to MAX				±10	μA	
I _{CC} Supply current from V _{CC}	I _O = 0 mA, T _A = 0°C (worst case)	TMS 2114 TMS 2114L	V _{CC} = MAX V _{CC} = MAX	90	100	50	60	mA
C _i Input capacitance	V _I = 0 V, f = 1 MHz					8	pF	
C _o Output capacitance	V _O = 0 V, f = 1 MHz					8	pF	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

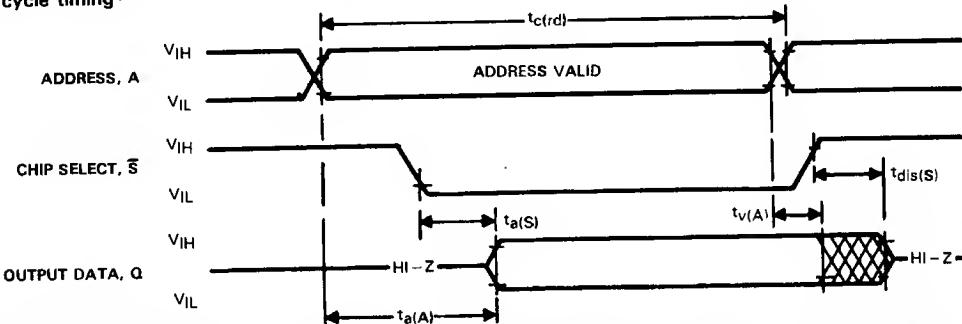
timing requirements over recommended supply voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load,
C_L = 100 pF

PARAMETER	TMS2114-15 TMS2114L-15		TMS2114-20 TMS2114L-20		TMS2114-25 TMS2114L-25		TMS2114-45 TMS2114L-45		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{c(rd)} Read cycle time	150	200			250		450		
t _{c(wr)} Write cycle time	150	200			250		450		ns
t _{w(W)} Write pulse width	80	100			100		200		ns
t _{su(A)} Address set up time	0	0			0		0		ns
t _{su(S)} Chip select set up time	80	100			100		200		ns
t _{su(D)} Data set up time	80	100			100		200		ns
t _{h(D)} Data hold time	0	0			0		0		ns
t _{h(A)} Address hold time	0	0			0		20		ns

switching characteristics over recommended voltage range, $T_A = 0^\circ\text{C}$ to 70°C , 1 Series 74 TTL
load, $C_L = 100 \text{ pF}$

PARAMETER	TMS2114-15		TMS2114-20		TMS2114-25		TMS2114-45		UNIT	
	TMS2114L-15		TMS2114L-20		TMS2114L-25		TMS2114L-45			
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_a(A)$	Access time from address	150	200	250	450				ns	
$t_a(S)$	Access time from chip select (or output enable) low	70	85	100	120				ns	
$t_a(W)$	Access time from write enable high	70	85	100	120				ns	
$t_v(A)$	Output data valid after address change	20	20	20	20				ns	
$t_{dis}(S)$	Output disable time after chip select (or output enable) high	50	60	60	100				ns	
$t_{dis}(W)$	Output disable time after write enable low	50	60	60	100				ns	

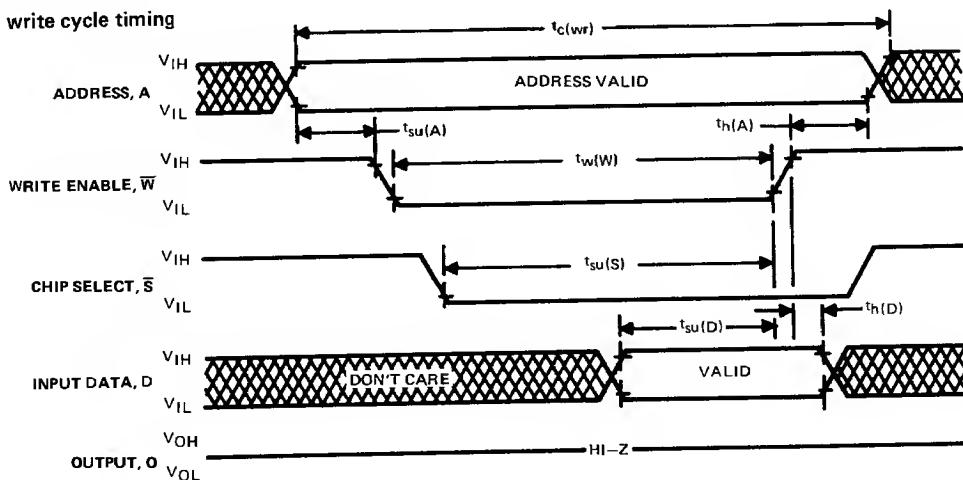
read cycle timing[†]



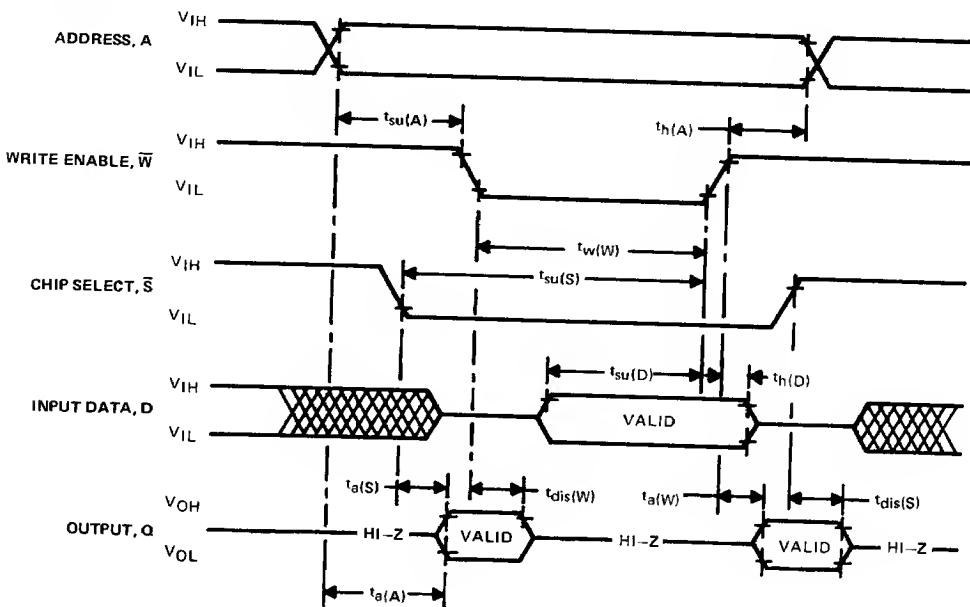
All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

[†]Write enable is high for a read cycle.

early write cycle timing



read-write cycle timing



TYPICAL APPLICATION DATA

Early write cycle avoids DQ conflicts by controlling the write time with \bar{S} . On the diagram above, the write operation will be controlled by the leading edge of \bar{S} , not \bar{W} . Data can only be written when both \bar{S} and \bar{W} are low. Either \bar{S} or \bar{W} being high inhibits the write operation. To prevent erroneous data being written into the array, the addresses must be stable during the write cycle as defined by $t_{su}(A)$, $t_w(W)$, and $t_h(A)$.

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.